What is claimed is:

1. A memory system comprising:

a memory controller having an interface that includes a plurality of memory subsystem ports including a first memory subsystem port;

a first memory subsystem including:

a buffer device having a first port and a second port, and

a plurality of memory devices coupled to the buffer device via the second port;

and

a plurality of point-to-point links, each point-to-point link having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of point-to-point links including a first point-to-point link connecting the first port to a first memory subsystem port to transfer data between the plurality of memory devices and the memory controller.

2. The memory system of claim 1 further including a plurality of connectors each connected to a connection to a respective point-to-point link and a plurality of memory subsystems, each memory subsystem of the plurality of memory subsystems including:

a buffer device having a first port and a second port, wherein the first port is coupled to a respective connector of the plurality of connectors , and

a plurality of memory devices coupled to the buffer device via the second port.

3. The memory system of claim 2 further including a plurality of substrates wherein each memory subsystem is disposed on a respective substrate of the plurality of substrates.

4. The memory system of claim 1 wherein each of the plurality of point-to-point links, first memory subsystem, and memory controller include a common substrate.

5. The memory system of claim 1 wherein the first memory subsystem further includes a plurality of channels and a plurality of memory device select lines connected between the plurality of memory devices and the second port.

6. The memory system of claim 5 wherein each channel includes a plurality of terminated signal lines.

7. The memory system of claim 1 wherein the buffer device of the first memory subsystem further includes at least one selected from the group consisting of a cache, a clock generator, and a clock alignment circuit.

8. The memory system of claim 1 further including a plurality of sideband signals coupled between the plurality of memory devices of the first memory subsystem and the controller device.

9. The memory system of claim 1 further including a plurality of sideband signals coupled between the plurality of buffer devices and the controller device.

10. A memory system comprising:

a controller device;

a first buffer device having a first interface and a second interface;

a second buffer device having a first interface and a second interface;

a first point-to-point link having a first connection to the controller device and a second connection to the first interface of the first buffer device;

a first channel connected to the second interface of the first buffer device;

a first plurality of memory devices electrically coupled to the first channel;

a second point-to-point link having a first connection to the controller device and a second connection to the first interface of the second buffer;

a second channel connected to the second interface of the second buffer device; and

a second plurality of memory devices electrically coupled to the second channel.

11. The memory system of claim 10, wherein the first buffer device, first channel and first plurality of memory devices are disposed on a first substrate, and the second buffer device, second channel, and second plurality of memory devices are disposed on a second substrate.

12. The memory system of claim 11, further including a plurality of termination elements disposed on each of the first and second substrate, wherein a first plurality of termination elements are connected to the first channel, and a second plurality of termination elements are connected to the second channel.

13. The memory system of claim 10, wherein the first buffer device further includes a third interface, the memory system further including:

a third buffer device having a first interface and a second interface;

a third point-to-point link having a first connection to the third interface and a second connection to the first interface of the third buffer device;

a third channel connected to the second interface of the third buffer device; and

a third plurality of memory devices electrically coupled to the third channel.

14. The memory system of claim 10 further including a third point-to-point link having a connection to the controller and a fourth point-to-point link having a connection to the controller.

15. The memory system of claim 10 further including:

a third channel connected to the second interface of the first buffer device;

a third plurality of memory devices electrically coupled to the third channel;

a fourth channel connected to the second interface of the second buffer device; and

a fourth plurality of memory devices electrically coupled to the fourth channel.

16. The memory system of claim 15 further including:

a fifth and sixth channel connected to the second interface of the first buffer device;

a fifth plurality of memory devices electrically coupled to the fifth channel; and

a sixth plurality of memory devices electrically coupled to the sixth channel.

17. The memory system of claim 10, further including at least one termination element disposed on the first buffer device and electrically connected to the first point-to-point link.

18. The memory system of claim 10 wherein the first and second buffer devices each further include at least one selected from the group consisting of a cache, a clock generator and a clock alignment circuit.

19. A memory system comprising:

a controller device;

a first and second plurality of buffer devices, each buffer device of the first and second plurality of buffer devices having an interface connected to a respective plurality of memory devices;

a first and second repeater device;

a first point-to-point link having a first connection to the controller device and a second connection to the first repeater device;

a second point-to-point link having a first connection to the controller device and a second connection to the second repeater device;

a first plurality of repeater links, each repeater link having a first connection to a respective buffer device of the first plurality of buffer devices, and a second connection to the first repeater device; and

a second plurality of repeater links, each repeater link having a first connection to a respective buffer device of the second plurality of buffer devices and a second connection to the second repeater device.

20. The memory system of claim 19, wherein each buffer device of the first and second plurality of buffer devices and corresponding plurality of memory devices are each disposed on a one of a plurality of respective module substrates.

21. The memory system of claim 19 further including a third point-to-point link having an end connected to the controller and a fourth point-to-point link having an end connected to the controller.

22. The memory system of claim 19 wherein each buffer device of the first and second plurality of buffer devices each further include at least one selected from the group consisting of a cache, a clock generator, and a clock alignment circuit.

23. A memory system comprising:

a controller device having an interface;

a first connector, second connector, and third connector;

a first point-to point link having a first connection to the interface and a second connection to the first connector;

a second point-to-point link having a first connection to the interface and a second connection to the second connector;

a third point-to-point link having a first connection to the interface and a second connection to the third connector; and

a first memory subsystem including:

a buffer device having a having a first interface connected to the first connector, and a second interface; and

a plurality of memory devices connected to the second interface.

24. The memory system of claim 23 wherein the second and third connectors support coupling to respective second and third memory subsystems.

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